IN THE CLAIMS

What is claimed id:

1. A semiconductor memory device having a SRAM in which a memory cell comprises a pair of transmission transistors and a flip-flop circuit containing a pair of driver transistors and a pair of load transistors, wherein:

a first interconnection formed from a first electrical conductor which is set on a semiconductor substrate, constitutes respective gate electrodes of said driver transistors, load transistors and transmission transistors;

a second interconnection including a second electrical conductor which is formed within a first trench that is set in a first insulating film lying on said semiconductor substrate, constitutes one of a pair of local interconnections cross-coupling a pair of input/output terminals in said flip-flop circuit;

a third interconnection which is formed on a second insulating film lying on a region including the top surface of said second interconnection, constitutes the other one of said pair of local interconnections; and

either said second interconnection or said third interconnection has a buried conductive section which is

formed to fill up the inside of said trench.

2. A semiconductor memory device according to Claim 1, wherein:

said second interconnection and said third interconnection have an overlapping section separated by said second insulating film; and

said second interconnection and said third interconnection, together with said second insulating film lying therebetween, constitute a capacitor element.

3. A semiconductor memory device according to Claim 1 or 2, wherein:

said second electrical conductor is disposed so as to come in contact with

a drain region constituting a first driver transistor which is one of said pair of driver transistors;

a drain region constituting a first load transistor which is one of said pair of load transistors and has a gate electrode formed from a first interconnection A, the gate electrode being in common to said first driver transistor; and

a first interconnection B which constitutes a gate electrode of a second driver transistor which is the other one of the pair of driver transistors as well

as a gate electrode of a second load transistor which is the other one of the pair of load transistors; and

said third interconnection is in contact with

a contact section connected to said first interconnection A;

a contact section connected to a drain region of said second driver transistor; and

a contact section connected to a drain region of said second load transistor.

4. A semiconductor memory device having a SRAM in which a memory cell comprises a pair of transmission transistors and a flip-flop circuit containing a pair of driver transistors and a pair of load transistors, wherein:

a first conductive film interconnection formed from a first conductive film which is set on a semiconductor substrate, constitutes respective gate electrodes of said driver transistors, load transistors and transmission transistors;

an inlaid interconnection set in a first insulating film lying on said semiconductor substrate, constitutes one of a pair of local interconnections cross-coupling a pair of input/output terminals in said flip-flop circuit; and

a second conductive film interconnection formed

from a second conductive film which is set on a second insulating film lying on said first insulating film, constitutes the other one of said pair of local interconnections.

5. A semiconductor memory device according to Claim 4, wherein

said second conductive film interconnection is disposed so as to overlap at least a portion of a top surface of said inlaid interconnection, with said second insulating film lying therebetween; and

said inlaid interconnection and said second conductive film interconnection, together with said second insulating film lying therebetween, constitute a capacitor element.

6. A semiconductor memory device according to Claim 5; wherein

said second conductive film interconnection is disposed so as to cover at least a portion of a lateral face of said inlaid interconnection, with said second insulating film placed therebetween; and

said inlaid interconnection and said second conductive film interconnection, together with said second insulating film lying therebetween, constitute a capacitor element.

7. A semiconductor memory device according to Claim 4, 5 or 6, wherein:

said inlaid interconnection is disposed so as to come in contact with

a drain region constituting a first driver transistor which is one of said pair of driver transistors;

a drain region constituting a first load transistor which is one of said pair of load transistors and has a gate electrode formed from a first conductive film interconnection A, the gate electrode being in common to said first driver transistor; and

a first conductive film interconnection B which constitutes a gate electrode of a second driver transistor which is the other one of the pair of driver transistors as well as a gate electrode of a second load transistor which is the other one of the pair of load transistors; and

said second conductive film interconnection is in contact with

a contact section to reach said first conductive film interconnection A;

a contact section to reach a drain region of said second driver transistor; and

a contact section to reach a drain region

of said second load transistor.

8. A semiconductor memory device according to Claim 7, wherein said first conductive film interconnection B branches off between the drain region of said second driver transistor and the drain region of said second load transistor, and this branched section of interconnection comes into contact with said inlaid interconnection.

9. A semiconductor memory device according to Claim 8, wherein a contact region between said branched section of interconnection and said inlaid interconnection contains a point that is, seen from the substrate top surface, equidistant from any among a group of said contact section to reach the first conductive film interconnection A, said contact section to reach the drain region of the second driver transistor, and said contact section to reach the drain region of the second load transistor.

10. A semiconductor memory device according to Claim 1, wherein:

said second interconnection comprises said buried conductive section which constitutes said second electrical conductor and a stacked electrode which is set

on said second electrical conductor;

said second insulating film covers said stacked electrode; and

said third interconnection is disposed on said second insulating film so as to overlap, at least, a portion of a top surface and a portion of a lateral face of said stacked electrode, and said stacked electrode and said third interconnection, together with said second insulating film lying therebetween, constitute a capacitor element.

11. A semiconductor memory device according to Claim 1, wherein:

said device further comprises a second trench which is formed in a third insulating film lying on said first insulating film;

said second interconnection comprises said buried conductive section which constitutes said second electrical conductor and a third electrical conductor which covers an inner side surface and a bottom surface of said second trench and has a first hollow in said second trench, said third electrical conductor contacting with an upper surface of said buried conductive section in the bottom of said second trench;

said second insulating film is formed on said third electrical conductor and has a second hollow in

said first hollow;

said third interconnection comprises a buried electrode which fills up said second hollow; and

said buried electrode and said third electrical conductor, together with said second insulating film lying therebetween, constitute a capacitor element.

12. A semiconductor memory device according to Claim 1, wherein:

said second electrical conductor covers an inner side surface and a bottom surface of said first trench and has a first hollow in said first trench;

said second insulating film is formed on said second electrical conductor and has a second hollow in said first hollow;

said third interconnection comprises said buried conductive section which fills up said second hollow; and

said second electrical conductor and said buried conductive section, together with said second insulating film lying therebetween, constitute a capacitor element.

13. A semiconductor memory device according to any one of Claims 1-12, wherein a refractory metal silicide layer is formed on the surface of every gate electrodes, source regions and drain regions of said pair of driver transistors, said pair of load transistors and

said pair of transmission transistors.

14. A method of manufacturing a semiconductor memory device having a SRAM in which a memory cell comprises a pair of transmission transistors and a flip-flop circuit containing a pair of driver transistors and a pair of load transistors, which comprises the steps of:

forming, on a semiconductor substrate, active regions to form respective source regions and drain regions of said driver transistors, said load transistors and said transmission transistors;

forming, on said semiconductor substrate, a first conductive film; and thereafter patterning this first conductive film to form a first conductive film interconnection that is to serve as an interconnection to constitute respective gate electrodes of said driver transistors, said load transistors and said transmission transistors;

forming, on said semiconductor substrate, a first insulating film; and thereafter forming, in this first insulating film, an inlaid interconnection as one of a pair of local interconnections cross-coupling a pair of input/output terminals in said flip-flop circuit; and

forming, on said first insulating film, a second insulating film, and thereafter forming a second conductive film and, then, patterning this second

conductive film to form a second conductive film interconnection as the other one of said pair of local interconnections.

15. A method of manufacturing a semiconductor memory device according to Claim 14, wherein

said second conductive film interconnection is disposed so as to overlap at least a portion of a top surface of said inlaid interconnection, with said second insulating film lying therebetween; and

said inlaid interconnection and said second conductive film interconnection, together with said second insulating film lying therebetween, constitute a capacitor element.

16. A method of manufacturing a semiconductor memory device having a SRAM in which a memory cell comprises a pair of transmission transistors and a flip-flop circuit containing a pair of driver transistors and a pair of load transistors, which comprises the steps of:

forming, on a semiconductor substrate, active regions to form respective source regions and drain regions of said driver transistors, said load transistors and said transmission transistors;

forming, on said semiconductor substrate, a first conductive film; and thereafter patterning this first

conductive film to form a first conductive film interconnection that is to serve as an interconnection to constitute respective gate electrodes of said driver transistors, said load transistors and said transmission transistors;

forming, on said semiconductor substrate, a first insulating film, and thereafter forming, in this first insulating film, an inlaid interconnection as one of a pair of local interconnections cross-coupling a pair of input/output terminals in said flip-flop circuit;

exposing a part of a lateral face of said inlaid interconnection; and

forming a second insulating film on said first insulating film and the exposed section of said inlaid interconnection; and thereafter forming a second conductive film and, then, patterning this second conductive film so as to overlap the top surface and a portion of the lateral face of said inlaid interconnection, with said second insulating film placed therebetween; and thereby forming a second conductive film interconnection which constitutes the other one of said pair of local interconnections, which provides a capacitor element composed of said second conductive film interconnection and the top surface and a portion of the lateral face of said inlaid interconnection, together with said second insulating film lying therebetween.

17. A method of manufacturing a semiconductor memory device according to Claim 14, 15 or 16, wherein:

said inlaid interconnection is formed so as to come in contact with

a drain region constituting a first driver transistor which is one of said pair of driver transistors;

a drain region constituting a first load transistor which is one of said pair of load transistors and has a gate electrode formed from a first conductive film interconnection A, the gate electrode being in common to said first driver transistor; and

a first conductive film interconnection B which constitutes a gate electrode of a second driver transistor which is the other one of the pair of driver transistors as well as a gate electrode of a second load transistor which is the other one of the pair of load transistors; and

said second conductive film interconnection is formed to come into contact with every one of contact sections which are made by forming, concurrently, a contact hole to reach said first conductive film interconnection A, a contact hole to reach the drain region of said second driver transistor, and a contact hole to reach the drain region of said second load

transistor; and thereafter filling up these contact holes with a conductive material.

18. A method of manufacturing a semiconductor memory device according to Claim 17, wherein said first conductive film interconnection B is formed into the branched shape in which branching off takes place between the drain region of said second driver transistor and the drain region of said second load transistor, and said inlaid interconnection is formed so as to come into contact with this branched section of interconnection.

19. A method of manufacturing a semiconductor memory device according to any one of Claims 14-18, which further comprises the step of forming a refractory metal silicide layer on the surface of every source regions and drain regions of said pair of driver transistors, said pair of load transistors and said pair of transmission transistors as well as on the surface of said first conductive film interconnection which constitutes gate electrodes thereof.